

FIG 1.

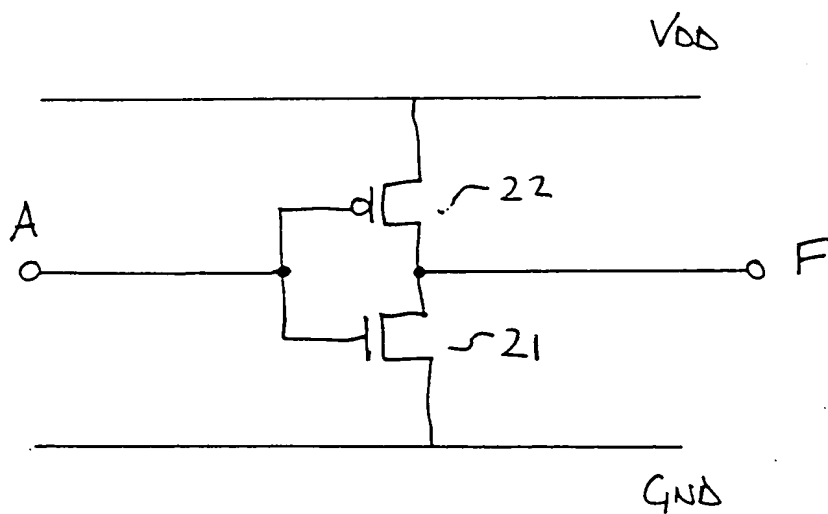


FIG 2.

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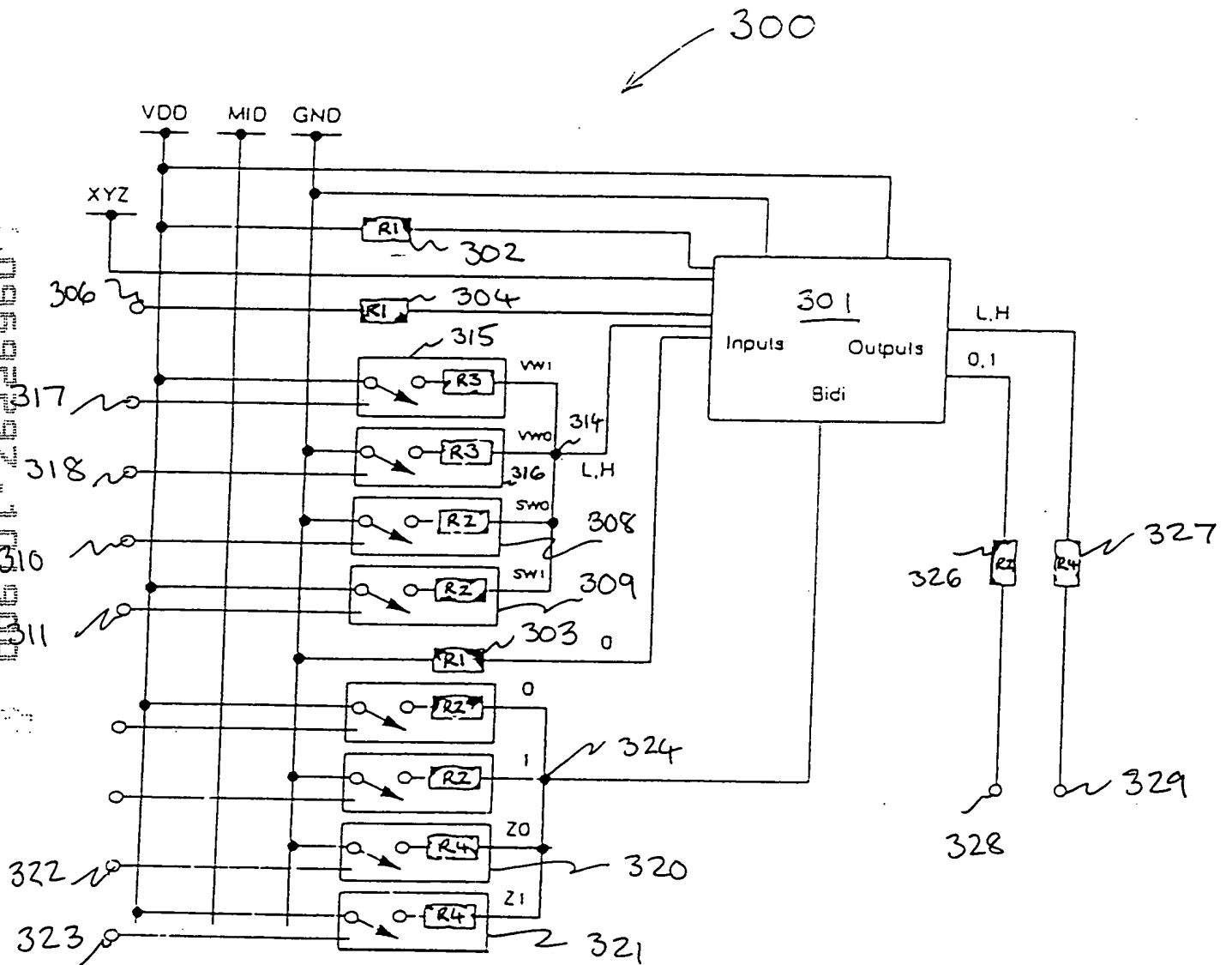


FIG 3.

400

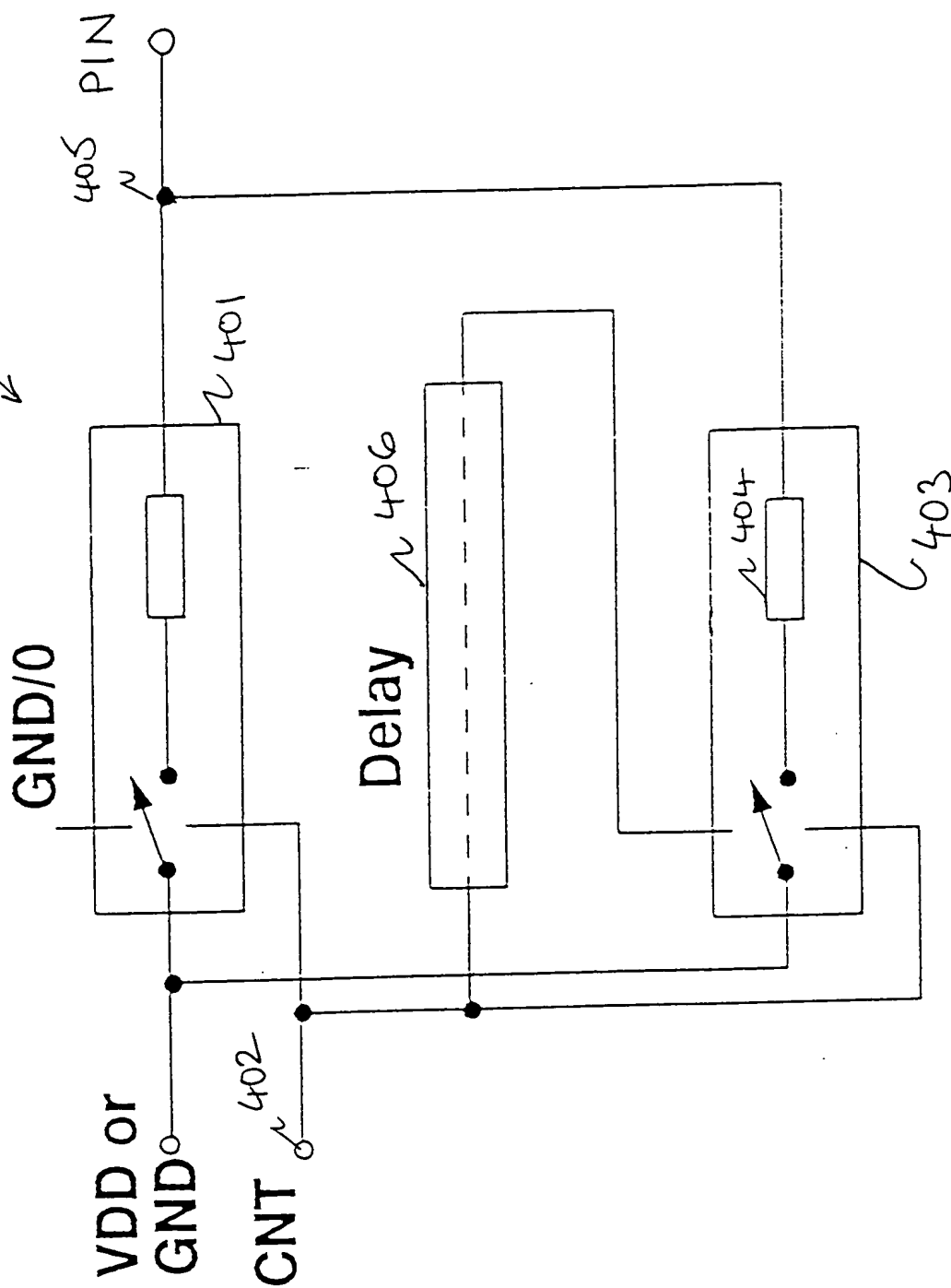


Fig 4.



FIG 5.

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$$F \cup R \in \mathcal{G}$$

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/-----\
|   start   |----- SI
\-----/

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/-----\ -52
| Read  WIF | DBmain = WIF data
\-----/

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----- 53  
 | Weaken BIDs | 0 = L, 1 = H, X = W  
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-----\ 54
Write out VHDL TB | VHDL = DBmain
Write control file | Tracing = none
-----/ Model in WORK cellname pack

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/-----\ ~55
| Analyse VHDL TB | VSS = VHDL
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Simulate VHDL	OW +? REAL = VSS
Convert Results	WIFhdl = OW +? REAL
Check Assertions	Stop if errors/known assertions

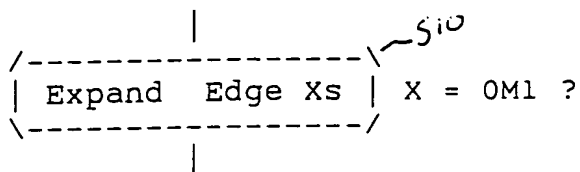
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      |
      | ~57
      |
      |-----|
      | Read WIF | DBslave = WIF data
      |-----|
  
```

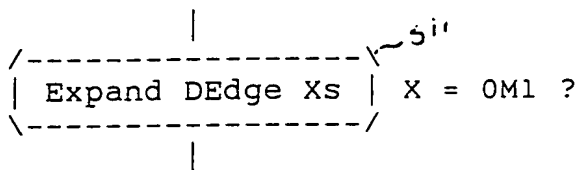
Copy O/P patterns DBmain(o/p) = DBslave(o/p)

Expand Level xs  $X = 0M1 ?$

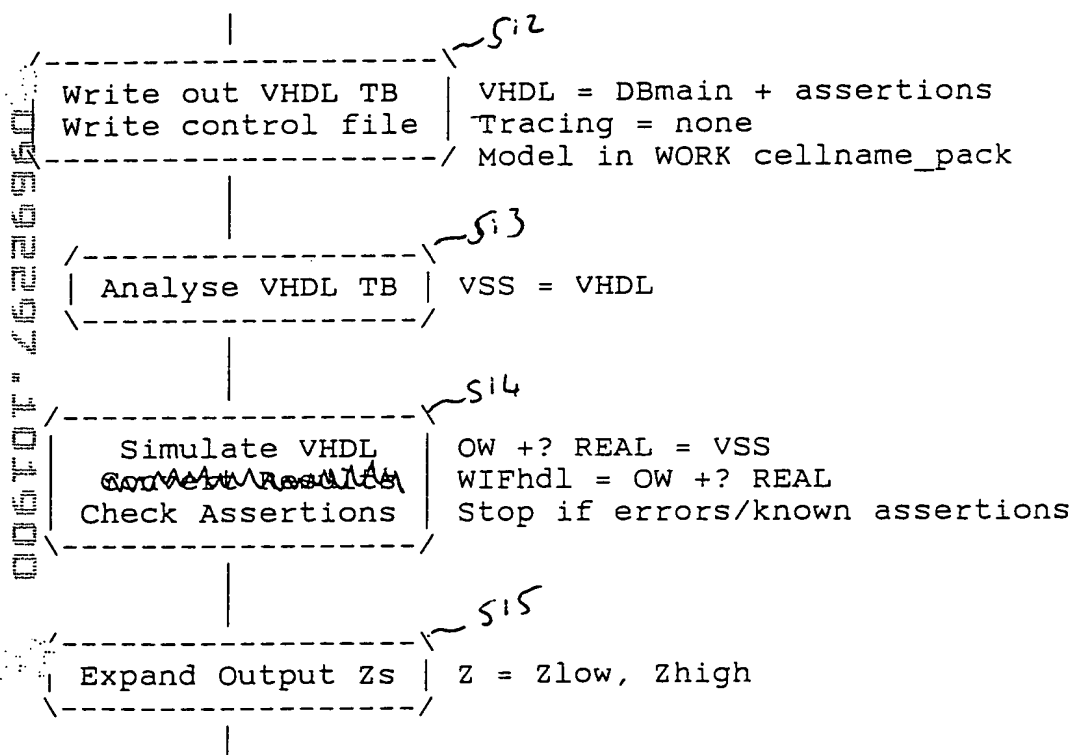
Stage 4 ----- Binary representation = 000100 ----- Stage 4



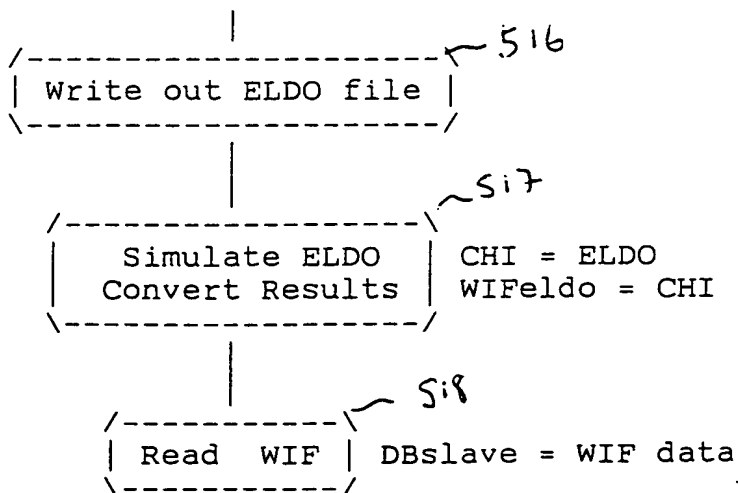
Stage 8 ----- Binary representation = 001000 ----- Stage 8



Stage 16 ----- Binary representation = 010000 ----- Stage 16



Stage 32 ----- Binary representation = 100000 ----- Stage 32



Verify ELDO  
Results

DBmain == DBslave  
for o/p using ELDO verifier

The End

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